IZBORNOM VEĆU ELEKTRONSKOG FAKULTETA U NIŠU

Predmet: Izveštaj Komisije o prijavljenom kandidatu za izbor u zvanje naučni savetnik

Izborno veće Elektronskog fakulteta u Nišu, odlukom broj 07/01-004/12-006 od 15.03.2012. godine, imenovalo je Komisiju za pisanje izveštaja o prijavljenom kandidatu za izbor u zvanje naučni savetnik (u daljem tekstu: Komisija) u sastavu:

1. dr Mile Stojčev, redovni profesor Elektronskog fakulteta u Nišu
2. dr Zoran Prijić, redovni profesor Elektronskog fakulteta u Nišu
3. dr Milun Jevtić, redovni profesor Elektronskog fakulteta u Nišu

Prihvatajući imenovanje i nakon detaljnog uvida u materijal, Komisija podnosi sledeći

I Z V E Š T A J

Dr Zoran Stamenković je podneo zahtev za izbor 05.07.2011. god. pod brojem 01/05-154/11 i priložio overenu kopiju diplome o stečenom akademskom zvanju doktora tehničkih nauka, biografiju, spisak radova i fotokopije radova. Komisija, nakon pregleda priložene dokumentacije, u nastavku izveštaja izneće sledeće relevantne podatke o kandidatu.

1. BIOGRAFSKI PODACI

1.1. Lični podaci

Dr Zoran Stamenković je rođen 28.01.1960. god. u Vranju. Živi i radi u Nemačkoj.

1.2. Podaci o dosadašnjem obrazovanju

Doktorsku disertaciju "Ekstrakcija kritičnih površina čipa pri modeliranju prinosa integrisanih kola" odbranio je 01.03.1995. god. na Elektronskom fakultetu u Nišu.

1.3. Profesionalna karijera

U zvanje vanredni profesor izabran je 28.06.2001. god. na Elektronskom fakultetu u Nišu za predmete Integrisani mikrosistemi i Hibridna integrisana kola. Naučni istraživač je Instituta za mikroelektroniku (IHP) u Frankfurtu na Odri, Nemačka. U svom dosadašnjem radu aktivno je učestvovao u realizaciji međunarodnih i nacionalnih naučno-istraživačkih projekata.

Oblast njegovog istraživačkog rada je projektovanje sistema na čipu za bežične komunikacije uključujući modeliranje hardvera, logičku sintezu, layout integrisanih kola, testiranje, i analiziranje prinosa i pouzdanosti.

Stalni je saradnik Katedre za tehničku informatiku Brandenburškog tehničkog univerziteta (BTU) u Cottbus-u i od 2009. god. drži nastavu iz predmeta “Mikroelektronika: Automatsko projektovanje digitalnih integrisanih kola” u letnjem semestru redovnih studija http://www.tu-cottbus.de/fakultaet1/de/technische-informatik/lehre/lehrangebot/aktuelles-semester.html.

2. PREGLED I MIŠLJENJE O NAUČNOM I STRUČNOM RADU KANDIDATA

Dr Zoran Stamenković je sam ili u saradnji sa drugim autorima, u okviru naučno-istraživačkog rada, napisao 77 naučno-istraživačkih radova. Ovde će biti navedeni i analizirani samo radovi objavljeni posle izbora u zvanje vanredni profesor.

2.1. Spisak naučnih radova publikovanih posle izbora u zvanje vanredni profesor

a) Poglavlje u istaknutoj monografiji međunarodnog značaja (M14):

a.1. **Z. Stamenković** and N. Stojadinović, "Computer-Aided Analysis and Forecast of Integrated Circuit Yield", Vojin G. Oklobdžija, Editor, Chapter in book "The Computer Engineering Handbook", CRC Press, Boca Raton, 2002, pp. 47.1-47.24, ISBN: 978-0-8493-0885-2, http://www.crcnetbase.com/isbn/9780849308857

a.2. U. Glaeser, **Z. Stamenković** and H. T. Vierhaus, "Testing of Synchronous Sequential Digital Circuits", Vojin G. Oklobdžija, Editor, Chapter in book "The Computer Engineering Handbook", CRC Press, Boca Raton, 2002, pp. 45.1-45.22, ISBN: 978-0-8493-0885-2, http://www.crcnetbase.com/isbn/9780849308857

a.3. H. T. Vierhaus and **Z. Stamenković**, "Test Technology for Sequential Circuits", Vojin G. Oklobdžija, Editor, Chapter in book "Digital Design and Fabrication", CRC Press, Boca Raton, 2008, pp. 22.1-22.14, ISBN: 978-0-8493-8602-2, http://www.crcnetbase.com/isbn/978-0-8493-8602-2

a.4. M. Mitić, M. Stojčev and **Z. Stamenković**, "An Overview of SOC Buses", Vojin G. Oklobdžija, Editor, Chapter in book "Digital Systems and Applications", CRC Press, Boca Raton, 2008, pp. 7.1-7.16, ISBN: 978-0-8493-8619-0, http://www.crcnetbase.com/isbn/978-0-8493-8619-0

a.5. T. Nikolić, M. Stojčev, G. Djordjević and **Z. Stamenković**, "Wrapper Design for CDMA Shared Bus in SOC", Thomas S. Clary, Editor, Chapter in book "Horizons in Computer Science Research", vol. 2, Nova Science Publishers Inc, New York, 2011, pp. 1-34, ISBN: 978-1-61761-439-2, https://www.novapublishers.com/catalog/product_info.php?products_id=17127

b) Rad u istaknutom međunarodnom časopisu (M22):

b.1. **Z. Stamenković**, K. Tittelbach-Helmrich, M. Krstić, J. Ibanez, V. Elvira and I. Santamaria, "MAC and Baseband Processors for RF-MIMO WLAN", EURASIP Journal on Wireless Communications and Networking, SpringerOpen, vol. 2011-207, pp. 1-13, December 2011, ISSN: 1687-1499, http://dx.doi.org/10.1186/1687-1499-2011-207

c) Rad u međunarodnom časopisu (M23):

c.1. **Z. Stamenković**, "SOC Design for Wireless Communications", Journal of Circuits, Systems, and Computers, World Scientific Publishing Co, vol. 20, no. 8, pp. 1505-1527, December 2011, ISSN: 0218-1266, http://dx.doi.org/10.1142/S0218126611008055

d) Rad u časopisu nacionalnog značaja (M52):

d.1. G. Jovanović, M. Stojčev and **Z. Stamenković**, "A CMOS Voltage Controlled Ring Oscillator with Improved Frequency Stability", Scientific Publications of the State University of Novi Pazar: Applied Mathematics, Informatics, and Mechanics, vol. 2, no. 1, pp. 1-9, May 2010, ISSN: 2217-5539, http://www.np.ac.rs/index.php/en/preuzimanjasve/vol2br1/182-a-cmos-voltage-controlled-ring-oscillator-with-improved-frequency-stability/download

d.2. G. Jovanović, M. Stojčev, T. Nikolić and **Z. Stamenković**, "Programmable Jitter Generator Based on Voltage Controlled Delay Line", Scientific Publications of the State University of Novi Pazar: Applied Mathematics, Informatics, and Mechanics, vol. 4, no.

1, pp. 61-73, March 2012, ISSN: 2217-5539, http://www.np.ac.rs/index.php/en/preuzimanjasve/vol4br1/776-vol4no1rad6/download

e) Predavanje po pozivu sa međunarodnog skupa štampano u celini (M31):

e.1. **Z. Stamenković**, "System-on-Chip Design: Engineering or Art", Proc. 25th International Conference on Microelectronics, Belgrade (Serbia), May 14-17, 2006, pp. 401-408, ISBN: 978-1-4244-0117-8, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=1650978

e.2. **Z. Stamenković**, "SOC Design for Wireless Communications", Proc. 12th Biennial Baltic Electronics Conference, Tallinn (Estonia), October 4-6, 2010, pp. 25-32, ISBN: 978-1-4244-7356-4, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5630885

e.3. **Z. Stamenković**, K. Tittelbach-Helmrich, M. Krstić, J. Ibanez, V. Elvira and I. Santamaria, "MAC and Baseband Hardware Platforms for RF-MIMO WLAN", Proc. 5th European Conference on Circuits and Systems for Communications, Belgrade (Serbia), November 23-25, 2010, pp. 26-33, ISBN: 978-1-6128-4400-8, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5733849

e.4. **Z. Stamenković**, K. Tittelbach-Helmrich, M. Wickert, J. Ibanez, S. Ruiz and G. Dimosthenous, "Implementation, Integration, and Verification of MIMAX WLAN Modem", Proc. 6th International Workshop on Reconfigurable Communication-Centric Systems-on-Chip, Montpellier (France), June 20-22, 2011, pp. 1-8, ISBN: 978-1-4577-0640-0, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5981523

e.5. **Z. Stamenković**, K. Tittelbach-Helmrich, R. Kraemer, S. Ruiz, O. Gago, J. Ibanez, I. Santamaria, M. Wickert and R. Eickhoff, "Circuits and Systems for RF-MIMO WLAN", Proc. 2nd International Symposium on Innovation and Technology, Lima (Peru), November 28-30, 2011, pp. 12-19, ISBN: 978-612-45917-1-6, http://iiitec.org

f) Predavanje po pozivu sa međunarodnog skupa štampano u izvodu (M32):

f.1. **Z. Stamenković**, "Testing and Yield of Integrated Circuits", 4th IEEE International Symposium on Quality Electronic Design, San Jose (USA), March 24-26, 2003, pp.1-45, http://www.isqed.org/English/Archives/2003/Program/trackB.htm

f.2. **Z. Stamenković**, "Configurable Processors for SOC Design", 5th IASTED International Conference on Circuits, Signals, and Systems, Banff (Canada), July 2-4, 2007, pp. 1-118, http://www.iasted.org/conferences/session-573.html

f.3. **Z. Stamenković**, "SOC Design and Configurable Processors", Chinese University of Hong Kong, Department of Electronic Engineering, Hong Kong (China) April 5-6, 2008, pp. 1-280, http://www.ee.cuhk.edu.hk/m_zoran.php

f.4. **Z. Stamenković**, "IHP as Access Point for West Balkan Students and Scientists in European ICT Research Programs", The eChallenges e-2010 Conference & Exhibition, Warsaw (Poland), October 27-29, 2010, pp. 1-10, http://www.echallenges.org/e2010/default.asp?page=schedule-print&schedule.id=244&schedule.expanded=yes

g) Saopštenje sa međunarodnog skupa štampano u celini (M33):

g.1. G. Panić, D. Dietterle, **Z. Stamenković** and K. Tittelbach-Helmrich, "A System-on-Chip Implementation of the IEEE 802.11a MAC Layer", Proc. 3rd EUROMICRO

Symposium on Digital System Design, Antalya (Turkey), September 1-6, 2003, pp. 319-324, ISBN: 978-0-7695-2003-0, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=1231962

g.2. **Z. Stamenković**, F. Vater and Z. Dyka, "A Framework for Selection of Cache Configurations for Low Power", Proc. 4th International Workshop on IP-Based System-on-Chip Design, Grenoble (France), November 13-14, 2003, pp. 137-140, http://www.design-reuse.com/articles/7319/a-framework-for-selection-of-cache-configurations-for-low-power.html

g.3. **Z. Stamenković**, G. Panić, U. Jagdhold, H. Frankenfeldt, K. Tittelbach-Helmrich, G. Schoof and R. Kraemer, "Modular Processor: A Flexible Library of ASIC Modules", Proc. 13th IASTED International Conference on Applied Simulation and Modelling, Rhodes (Greece), June 28-30, 2004, pp. 428-432, ISBN: 978-0-8898-6397-0, http://www.actapress.com/Abstract.aspx?paperId=18686

g.4. G. Panić, **Z. Stamenković**, K. Tittelbach-Helmrich, J. Lehmann and G. Schoof, "Design of Wireless Systems Utilizing Scratchpad Memories", Proc. 6th IP-Based System-on-Chip Design Conference, Grenoble (France), December 7-8, 2005, pp. 221-226, http://www.design-reuse.com/articles/13761/design-of-wireless-systems-utilizing-scratchpad-memories.html

g.5. **Z. Stamenković**, C. Wolf, G. Schoof and J. Gaisler, "LEON-2: General Purpose Processor for a Wireless Engine", Proc. 9th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, Prague (Czechia), April 18-21, 2006, pp. 50-53, ISBN: 978-1-4244-0184-4, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=1649569

g.6. **Z. Stamenković**, C. Wolf, G. Schoof and J. Gaisler, "An Implementation Study on Fault Tolerant LEON-3 Processor System", Proc. 7th IP-Based System-on-Chip Design Conference, Grenoble (France), December 6-7, 2006, pp. 23-26, http://www.us.design-reuse.com/articles/article15502.html

g.7. **Z. Stamenković**, D. Dietterle, G. Panić, W. Bocer, G. Schoof and J.-P. Ebert, "MAC Processor for BASUMA Wireless Body Area Network", Proc. 5th IASTED International Conference on Circuits, Signals, and Systems, Banff (Canada), July 2-4, 2007, pp. 47-52, ISBN: 978-0-8898-6669-0, http://www.actapress.com/Abstract.aspx?paperId=30881

g.8. **Z. Stamenković**, G. Panić and G. Schoof, "A System-On-Chip for Wireless Body Area Sensor Network Node", Proc. 11th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, Bratislava (Slovakia), April 16-18, 2008, pp. 132-135, ISBN: 978-1-4244-2276-0, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=4538770

g.9. G. Panić, **Z. Stamenković** and R. Kraemer, "Power Gating in Wireless Sensor Networks", Proc. 3rd IEEE International Symposium on Wireless Pervasive Computing, Santorini Island (Greece), May 7-9, 2008, pp. 499-503, ISBN: 978-1-4244-1652-3, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=4556258

g.10. G. Panić, D. Dietterle and **Z. Stamenković**, "Architecture of a Power-Gated Wireless Sensor Node", Proc. 11th IEEE EUROMICRO Conference on Digital System Design, Parma (Italy), September 3-5, 2008, pp. 844-849, ISBN: 978-0-7695-3277-6, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=4669324

g.11. **Z. Stamenković**, M. Giles and F. Russi, "Combining Internal Scan Chains and Boundary Scan Register: A Case Study", Proc. IEEE Region 8 EUROCON 2009 Conference, Saint Petersburg (Russia), May 18-23, 2009, pp. 2064-2069, ISBN: 978-1-4244-3860-0, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5167932

g.12. **Z. Stamenković**, K. Tittelbach-Helmrich, M. Krstić, J. Perez, J. Via and J. Ibanez, "Architecture of an Analog Combining MIMO System Compliant to IEEE802.11a", Proc. ICT-MobileSummit 2009, Santander (Spain), June 10-12, 2009, pp. 1-8, ISBN: 978-1-9058-2412-0, http://www.ict-mobilesummit.eu/2009/default.asp?page=schedule-print&schedule.id=69&schedule.expanded=yes

g.13. **Z. Stamenković**, E. Miletić, M. Obrknežev and K. Tittelbach-Helmrich, "MAC Protocol Implementation in RF-MIMO WLAN", Proc. 16th IEEE International Conference on Electronics, Circuits, and Systems, Yasmine Hammamet (Tunisia), December 13-16, 2009, pp. 303-306, ISBN: 978-1-4244-5090-9, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5410996

g.14. T. Nikolić, M. Stojčev and **Z. Stamenković**, "Wrapper Design for a CDMA Bus in SOC", Proc. 13th IEEE International Symposium on Design and Diagnostics of Electron Circuits and Systems, Vienna (Austria), April 14-16, 2010, pp. 243-248, ISBN: 978-1-4244-6610-8, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5491774

g.15. M. Erić, G. Panić and **Z. Stamenković**, "LEON2 Processor with High-Speed USB Port: A System-On-Chip for Wireless Applications", Proc. 27th International Conference on Microelectronics, Niš (Serbia), May 16-19, 2010, pp. 357-360, ISBN: 978-1-4244-7200-0, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5490466

g.16. K. Tittelbach-Helmrich, E. Miletić, P. Wcislek and **Z. Stamenković**, "MAC Hardware Platform for RF-MIMO WLAN", Proc. 53rd IEEE International Midwest Symposium on Circuits and Systems, Seattle (USA), August 1-4, 2010, pp. 339-342, ISBN: 978-1-4244-7771-5, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5548838

g.17. R. Kraemer, **Z. Stamenković**, K. Tittelbach-Helmrich, L. Gonzalez, S. Ruiz, O. Gago, J. Ibanez, V. Elvira, M. Wickert and R. Eickhoff, "RF-MIMO WLAN Modem Demonstrator", Proc. 25th Wireless World Research Forum Meeting, London (United Kingdom), November 16-18, 2010, pp. 1-10, http://typo3.wireless-world-research.org/fileadmin/sites/default/files/meetings/NextMeetings/WWRF25/WWRF25_agenda_vers9.pdf

g.18. V. Elvira, J. Ibanez, I. Santamaria, M. Krstić, K. Tittelbach-Helmrich and **Z. Stamenković**, "Baseband Processor for RF-MIMO WLAN", Proc. 17th IEEE International Conference on Electronics, Circuits, and Systems, Athens (Greece), December 12-15, 2010, pp. 798-801, ISBN: 978-1-4244-8155-2, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5724633

g.19. U. Pešović, S. Randjić and **Z. Stamenković**, "A Wireless ECG Sensor Node Based on Huffman Data Encoder", Proc. 14th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems, Cottbus (Germany), April 13-15, 2011, pp. 411-412, ISBN: 978-1-4244-9755-3, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5783126

g.20. R. Eickhoff, K. Tittelbach-Helmrich, M. Wickert, J. Wagner, U. Mayer, V. Elvira, J. Ibanez, **Z. Stamenković** and F. Ellinger, "Physical Layer Amendments for MIMO Features in 802.11a", Proc. Future Network and Mobile Summit 2011, Warsaw

(Poland), June 15-17, 2011, pp. 1-8, ISBN: 978-1-4577-0928-9, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=6095231

g.21. V. Petrović, M. Ilić, G. Schoof and **Z. Stamenković**, "Design Methodology for Fault Tolerant ASICs", 15th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems, Tallinn (Estonia), April 18-20, 2012, http://ddecs2012.ati.ttu.ee/files/DDECS_Program.pdf

g.22. **Z. Stamenković**, K. Tittelbach-Helmrich, J. Domke, C. Lörchner-Gerdaus, J. Anders, V. Sark, M. Erić and N. Šira, "Rear View Camera System for Car Driving Assistance", 28th International Conference on Microelectronics, Niš (Serbia), May 13-16, 2012, http://miel.elfak.ni.ac.rs/fajlovi/Preliminary_%20Programme_2012.pdf

g.23. G. Jovanović, M. Stojčev, T. Nikolić and **Z. Stamenković**, "Clock Jitter Generator with Picoseconds Resolution", 28th International Conference on Microelectronics, Niš (Serbia), May 13-16, 2012, http://miel.elfak.ni.ac.rs/fajlovi/Preliminary_%20Programme_2012.pdf

h) Saopštenje sa međunarodnog skupa štampano u izvodu (M34):

h.1. Z. Stamenković, M. Giles and F. Russi, "Scan-Through-TAP: Combining Scan Chain and Boundary Scan Features in SOC", 13th IEEE European Test Symposium, Vendor Session, Lago Maggiore (Italy), May 25-29, 2008, pp. 1-10, http://www.cad.polito.it/~ets08/program.html

i) Realizovani patent (M91):

i.1. R. Kraemer, M. Krstić, Z. Stamenković, K. Tittelbach-Helmrich, I. Santamaria, J. Via, J. Perez and J. Ibanez, MIMO Transmission in IEEE802.11 WLAN Systems, European Patent Application EP2234355, 2010, http://www.freepatentsonline.com/EP2234355.html

2.2. Analiza naučnih radova publikovanih posle izbora u zvanje vanredni profesor

Dr Zoran Stamenković je autor ili koautor 77 naučno-istraživačkih radova. Pored doktorske disertacije i magistarske teze, pre izbora u zvanje vanredni profesor, objavio je jednu monografiju nacionalnog značaja, 7 radova u međunarodnim časopisima, 11 radova na međunarodnim konferencijama i 14 radova na nacionalnim konferencijama.

Posle izbora u zvanje vanredni profesor, dr Zoran Stamenković je objavio 42 rada u monografijama, časopisima i na međunarodnim konferencijama i simpozijumima. Objavljeni radovi i celokupna naučno-istraživačka delatnost su iz oblasti mikroelektronike i projektovanja sistema na čipu. Kandidat ima pet monografskih poglavlja u tematskim zbornicima međunarodnog značaja (M14), dva rada sa SCI liste koji su publikovani u međunarodnim časopisima (M22 i M23), dva rada u časopisu nacionalnog značaja (M52), pet predavanja po pozivu sa međunarodnog skupa štampana u celini (M31), četiri predavanja po pozivu sa međunarodnog skupa štampana u izvodu (M32), dvadeset tri rada sa međunarodnih skupova štampana u celini (M33), i jedan rad sa međunarodnog skupa štampan u izvodu (M34). Koautor je jednog evropskog patenta. Rad **f.4** prezentira rezultate međunarodne naučne saradnje IHP-a sa akademskim institucijama zemalja Zapadnog Balkana u okviru nacionalnih i evropskih istraživačkih projekata. Ostali radovi će biti analizirani po srodnosti tematike koju obrađuju i mogu se svrstati u pet kategorija.

U prvu kategoriju spadaju radovi **a.1**, **a.2**, **a.3**, **f.1**, **g.11** i **h.1** koji su posvećeni različitim aspektima testiranja integrisanih kola i modeliranja i predviđanja prinosa integrisanih kola. Druga kategorija radova (**d.1**, **d.2**, **g.3**, **g.21** i **g.23**) pripada oblasti projektovanja digitalnih i

analognih aplikaciono specifičnih integrisanih kola (ASIC). Treću kategoriju čine radovi **a.4**, **a.5**, **c.1**, **e.1**, **e.2**, **f.2**, **f.3**, **g.2**, **g.6**, **g.12**, **g.13**, **g.14** i **g.20** koji obrađuju arhitekturu i komponente sistema na čipu, kao i hardver/softver kodizajn. Radovi iz četvrte kategorije (**g.4**, **g.5**, **g.7**, **g.8**, **g.9**, **g.10**, **g.15** i **g.19**) posvećeni su projektovanju i realizaciji sistema na čipu male potrošnje, pre svega za bežične senzorske mreže (WSN). Petu kategoriju čine radovi **b.1**, **e.3**, **e.4**, **e.5**, **g.1**, **g.16**, **g.17**, **g.18** i **g.22** koji razmatraju različite aspekte projektovanja i realizacije sistema na čipu za širokopojasne bežične mreže kratkog dometa (WLAN).

Radovi **a.1** i **f.1** razmatraju modeliranje i predviđanje prinosa integrisanih kola. Predložen je model za upravljanje prinosom integrisanih kola koji ima za cilj otkrivanje najkritičnijih procesnih koraka. Predloženi model daje srednju vrednost i varijansu prinosa pločice za svaki kritični proces, što omogućava procenu ekonomske opravdanosti proizvodnje pojedinih tipova integrisanih kola. Osim toga, radovi sadrže originalne naučne priloge koji se odnose na modeliranje i ekstrakciju kritičnih površina čipa pomoću računara. Predloženi su novi modeli za ocenu kritičnih površina čipa za tačkaste i litografske defekte. Predložen je originalni metod za lokalnu ekstrakciju kritičnih površina čipa i razrađen algoritam za ekstrakciju površina preklapanja i algoritam za ekstrakciju kritičnih površina za litografske defekte. Razvijen je softverski sistem PRELAY/EXACCA/GRAPH za vizuelno prikazivanje kritičnih površina.

Rad **a.2** sadrži originalne naučne doprinose kandidata iz oblasti testiranja digitalnih integrisanih kola i sistema. U njemu je predložen novi pristup za testiranje sekvencijalnih digitalnih integrisanih kola i opisana tehnika genetske manipulacije i modeliranja otkaza. Generisanje testnih vektora se obavlja hijerarhijski na dva nivoa: switch-nivou i gate-nivou. Veza izmedju različitih nivoa se ostvaruje pomoću specijalnih interfejsa (backtracks) čiji je broj minimiziran korišćenjem jednostavne heuristike za identifikaciju ograničenja. Novi pristup i razvijeni algoritam (FOGBUSTER) za hijerarhijsko generisanje testova se zasnivaju na “forward-propagation backward-initialization” tehnici. Primenom četvorovrednosne logike i dvostepenog “backtracking” mehanizma rešen je “over-specification” problem i postignuta kompletnost testiranja. Algoritam je implementiran i integrisan u automatski generator testnih vektora SEMILET. Eksperimentalni rezultati generisanja testnih vektora za standardna integrisana kola ISCAS '85 i ISCAS '89 pokazuju da predloženi pristup i FOGBUSTER algoritam poseduju, u proseku, znatno bolje karakteristike od tradicionalnog HITEC pristupa i BACK algoritma.

Pregledni rad **a.3** opisuje standardne DFT (Design for Testability) tehnike u oblasti sekvencijalnih integrisanih kola i sistema na čipu kao što su “full-scan test” i “partial-scan test” tehnike. Osim toga, prezentirane su opšte karakteristike savremenih ATPG (Automatic Test Pattern Generation) tehnika i softverskih paketa za njihovu realizaciju. Posebna pažnja je posvećena tehnici detektovanja dinamičkih otkaza u kombinacionim kolima.

U radovima **g.11** i **h.1** kandidat prezentira originalnu DFT tehniku za testiranje sistema na čipu koja kombinuje unutrašnje scan elemente (flip-flop-ove) sa perifernim scan registrom u jedinstveni STT (Scan-Through-TAP) registar. Ova tehnika omogućava pristup unutrašnjim elementima kola sa sistemskog nivoa preko testnih pinova (Test Access Ports) korišćenjem standardne IEEE 1149.1 instrukcije.

Rad **d.1** razmatra originalni dizajn naponsko kontrolisanog ring oscilatora baziranog na N-stage single-ended nizu različitih tipova invertora u 1.2 μm CMOS tehnologiji. Predloženi ring oscilator poseduje povećanu stabilnost frekvencije oscilovanja u poređenju sa standardnim rešenjima i u odnosu na promene temperature ($\Delta f / f < 2$ %) i u odnosu na promene napona napajanja ($\Delta f / f < 4$ %). Ekstrakcija električnih parametara ring oscilatora je izvršena pomoću HSpice simulacija.

U radu **g.3** je opisan specifičan pristup ASIC projektovanju, koji ima za cilj kreiranje biblioteke ASIC modula koji su hijerarhijski uređeni i pogodni za višestruko korišćenje u

standardnom ciklusu projektovanja digitalnih sistema na čipu. Posebna pažnja je posvećena specifikaciji, sintezi, layout-u i verifikaciji ASIC modula za bežične komunikacije.

Rad **g.21** predstavlja modifikovanu metodologiju projektovanja fault-tolerant ASIC-a otpornih na SEU (Single Event Upset) otkaze u sekvencijalnim kolima, SET (Single Event Transient) otkaze u kombinacionim kolima, kao i SEL (Single Event Latchup) otkaze u svim CMOS kolima. Osnovu novog pristupa čine DMR (Dual Modular Redundancy) tehnika i SEL tranzistor-prekidač koji aktivira/deaktivira linije za napajanje. Prezentirani rezultati merenja i simulacija 1000-bitnog pomeračkog registra jasno ističu prednosti DMR tehnike u poređenju sa tradicionalnom TMR (Triple Modular Redundancy) tehnikom u pogledu postignutog nivoa zaštite, potrošnje energije i potrebne površine čipa. Treba naglasiti da je u ovom radu po prvi put prezentirana i realizovana metodologija zaštite CMOS integrisanih kola od sve tri vrste otkaza (SEU, SET i SEL) koji nastaju u uslovima pojačanog zračenja.

U radovima **d.2** i **g.23** je opisano projektovanje i implementacija originalnog analogno-digitalnog programabilnog džiter-generatora koji se koristi za procenu performansi sitema. Džiter-generator je realizovan pomoću naponski kontrolisane digitalne linije za kašnjenje (coarse-grain jitter) i analognog linearnog elementa za kašnjenje (fine-grain jitter). Predloženom metodom moguće je generisati različite komponente džitera i dodati ih ulaznom nizu podataka ili taktnom signalu.

Pregledni rad **a.4** kritički sistematizuje najpopularnije bus-arhitekture za internu komunikaciju u sistemima na čipu. Diskutovane su prednosti i nedostaci AMBA, Avalon, CoreConnect, STBus i Wishbone bus-arhitektura s obzirom na topologiju, metod arbitriranja, digitalnu širinu i način prenosa podataka. Posebna pažnja je posvećena problemima izbora bus-arhitekture u zavisnosti od potrebne brzine i načina prenosa podataka uslovljenih izborom IP komponenata.

U radovima **a.5** i **g.14** razmatraju se savremeni sistemi na čipu koje čini veliki broj integrisanih IP (Intellectual Property) komponenata. Istraživanja su usmerena ka projektovanju efikasne komunikacione arhitekture na čipu zasnovane na CDMA tehnici prenosa. Glavni doprinos ove tehnike odnosi se na smanjenje broja linija sistemske magistrale koje iznosi od 25% do 81%, dok je nedostatak povećana latencija u toku očitavanja i upisivanja podataka. Četiri različite strukture wrapper-a (linije magistrale su grupisane u bundle-ove od 4, 8, 16 ili 32 linije), koji predstavlja interfejs između IP blokova i deljive magistrale, opisane su VHDL-om i implementirane kao FPGA (Xilinx tehnologija) i ASIC (IHP 0.25 μm CMOS tehnologija). Rezultati pokazuju da je za implementaciju master-slave para wrapper-a potrebno oko 2000 gejtova, dok je za razmatrani CPU potrebno oko 30000 gejtova, što znači da je povećanje hardvera manje od 8%.

Pregledni radovi **c.1, e.1** i **e.2** predstavljaju celovitu i iscrpnu analizu metoda za projektovanje, arhitektura i komponenata sistema na čipu za bežične komunikacije. Oni opisuju osnove projektovanja visokointegrisanih digitalnih mikrosistema male snage čija složenost raste eksponencijalno, kao i potrebni resursi za njihovo projektovanje. Metodologija projektovanja sistema na čipu se zasniva na preciznoj specifikaciji sistema, višestrukom korišćenju procesorskih modula i ranom otkrivanju eventualnih grešaka. Radovi detaljno analiziraju i povezuju ove teme, počevši od opisa, preko verifikacije i realizacije, do testiranja tri sistema na čipu za tri različita standarda (IEEE 802.11, IEEE 802.15.3 i IEEE 802.15.4) u oblasti bežičnih komunikacija. Projektovani i realizovani sistemi su bazirani na konfigurabilnim i ekstenzibilnim procesorima opšte namene, specijalizovanim hardverskim akceleratorima za komunikacione namene i embedid-memorijama.

Radovi **f.2** i **f.3** obradjuju tematiku savremenih konfigurabilnih i ekstenzibilnih processora koji mogu biti brzo i lako prilagođeni odgovarajućoj korisničkoj nameni. Detaljno su analizirane arhitekture konfigurabilnih procesora male potrošnje (MIPS32, Xtensa, LEON2 i

LEON3) i njihova konfiguraciona okruženja. Ilustrovano je korišćenje konfigurabilnih procesora u procesu projektovanja sistema na čipu za bežične komunikacije na nekoliko primera.

U radu **g.2** je opisana i primenjena originalna tehnika za izbor procesorskih instrukcionih i data keš memorijskih konfiguracija koje obezbeđuju minimalnu potrošnju energije na nivou sistema. Tehnika se zasniva na definisanju novog parametra za karakterizaciju potrošnje koji predstavlja proizvod ocenjene verovatnoće promašaja pri čitanju keša i memorijskog kapaciteta keša. Posebno je istraživan uticaj asociativnosti keša na potrošnju energije i, na osnovu toga, predložena optimalna konfiguracija instrukcionog i data keša MIPS4KEp procesora za zadatu aplikaciju.

Rad **g.6** razmatra implementacione aspekte fault-tolerant LEON3 procesorskog sistema na čipu projektovanog za upotrebu u svemirskim tehnologijama. Sistem je otporan na SEU otkaze zahvaljujući implementiranoj TMR (Triple Modular Redundancy) zaštiti flip-flop-ova i EDAC (Error Detection And Correction) zaštiti SRAM-ova. Visoka testabilnost sistema je obezbeđena primenom “full-scan test” tehnike.

Rad **g.12** opisuje arhitekturu novog RF-MIMO (Radio Frequency Multiple Input Multiple Output) sistema i arhitekture njegovih baseband and MAC (Medium Access Control) podsistema. Ovaj sistem, za razliku od tradicionalnih MIMO sistema, obavlja obradu radio-signala (beamforming) u RF-domenu. Posebno su istaknuti istraživački rezultati postignuti u razvoju algoritama za estimaciju radio-kanala i selekciju težinskih (beamforming) koeficijenata. Komparativna analiza simulacionih rezultata BER (Bit Error Rate) parametra i složenosti hardvera pokazuje da RF-MIMO sistem poseduje bolje karakteristike od standardnih SISO (Single Input Single Output) i MIMO (Multiple Input Multiple Output) sistema.

Rad **g.13** prezentira modifikacije i ekstenzije IEEE 802.11 MAC (Medium Access Control) protokola koje nameće predložena RF-MIMO arhitektura. Razvijen je kompletan SDL (Specification and Description Language) model za simulaciju MAC protokola koji omogućava efikasnu implementaciju i podelu protokola na hardver i softver (hardware-software codesign).

Rad **g.20** opisuje pristup i rezultate istraživanja koji su omogućili korišćenje MIMO tehnologije u WLAN (Wireless Local Area Network) sistemima čiji standardni IEEE 802.11a PHY protokol ne podržava MIMO komunikaciju. Novi pristup je baziran na diverziti-tehnici kombinovanja signala u RF frontend-u pomoću vektor-modulatora u predajniku i prijemniku. Optimalne vrednosti težinskih (beamforming) koeficijenata izračunavaju baseband algoritmi na bazi estimacije odziva MIMO kanala. Predloženi pristup obezbeđuje efikasniji i pouzdaniji PHY protokol i njegovu kompatibilnost sa IEEE 802.11a standardom.

U radovima **g.4** i **g.5** kandidat razvija koncept korišćenja scratchpad-memorija i keš-memorija u sistemima na čipu male snage. Koncept je ilustrovan na primeru projektovanja i realizacije sistema na čipu za razvoj i testiranje hardvera i softvera u oblasti bežičnih komunikacija. Jedan sistem je baziran na AMBA basu i MIPS4KEp procesoru koji uključuje instrukcione i data scratchpad-memorije. Drugi sistem je baziran na AMBA basu i LEON2 procesoru koji uključuje instrukcione i data keš-memorije. Prednosti sistema sa scratchpad-memorijama u odnosu na sistem sa keš-memorijama su manja potrošnja energije i manja ukupna površina čipa. Međutim, u slučaju sistema sa scratchpad-memorijama je potrebno razviti softver koji će efikasno koristiti raspoložive memorijske resurse.

Radovi **g.7** i **g.8** sadrže naučne doprinose kandidata u oblasti projektovanja, implementacije i verifikacije sistema na čipu u ASIC tehnologiji namenjenih razvoju MAC protokola za dva komunikaciona standarda u oblasti bežičnih mreža veoma kratkog dometa (WPAN). Prvi sistem na čipu implementira MAC protokol IEEE 802.15.3 standarda i razvijen je za medicinske potrebe (praćenje vitalnih funkcija pacijenata pomoću senzora). Primenom hardver-softver kodizajna i hardverskog akceleratora za izvršenje kritičnih operacija, postignuto je značajno ubrzanje MAC protokola. Ovaj sistem sadrži i integrisanu fleš-memoriju za sistem-

ski firmver. Drugi sistem na čipu realizuje MAC protokol IEEE 802.15.4 standarda koji nameće izuzetno stroge zahteve u pogledu potrošnje energije. Iz tog razloga, razvijen je 16-bitni IPMS430 procesor veoma male snage (klon Texas Instruments MSP430 procesora) u saradnji sa Fraunhofer institutom.

Radovi **g.9** i **g.10** opisuju originalne power-saving tehnike i power-gating mehanizme za redukciju statičkih gubitaka energije u sistemima na čipu za bežične senzorske mreže. Prekid napajanja (power-gating) pojedinih funkcionalnih blokova senzor-noda se obavlja uz pomoć power-management jedinice (finite-state-machine) i tranzistorskih prekidača (power-gates). Predloženi pristup i arhitektura senzor-noda su verifikovani na testnom čipu koji sadrži processor opšte namene, kripto-procesor, priprocesor i MAC hardver akcelerator. Osim toga, istraživani su efekti primene power-gating tehnike u senzor-nodu veoma niske aktivnosti. Pokazano je da u tom slučaju power-gating obezbeđuje uštedu od oko 50 % ukupne potrošnje energije.

Radovi **g.15** i **g.19** sadrže rezultate projektovanja, implementacije i verifikacije sistema na čipu u FPGA tehnologiji namenjenih razvoju MAC protokola i tehnika za kontrolu i kompresiju podataka u bežičnim senzorskim mrežama male snage. Sistemi koriste različite procesore opšte namene (LEON2 i ARM Cortex) i standardne serijske portove (USB i UART).

Radovi **b.1**, **e.3**, **g.16** i **g.18** opisuju IEEE 802.11 MAC (Medium Access Control) protokol i digitalni baseband jednog RF-MIMO WLAN primopredajnika koji obavlja obradu radio-signala (beamforming) u analognom domenu. Posebni trening-frejmovi omogućavaju izračunavanje optimalnih beamforming-koeficijenata za bilo koju i svaku radio-vezu u lokalnoj mreži. Trening-faze kontroliše modifikovani IEEE 802.11 MAC protokol. Glavni doprinos opisanih istraživanja je nova arhitektura MAC procesora koji uključuje hardverski akcelerator i 16-bitni MAC-PHY interfejs. Predloženo rešenje je testirano i verifikovano korišćenjem PHY emulatora. Osim toga, predložena je nova arhitektura rekonfigurabilnog baseband procesora i razvijeni novi baseband algoritmi za estimaciju MIMO kanala i kombinovanje signala na predajnoj i prijemnoj strani. Opisana je FPGA realizacija novih arhitektura, integrisani PCB sistem i rezultati testiranja sistema u realnom vremenu. Novi MAC procesor obezbeđuje brži protok podataka i pouzdaniju radio-vezu od prethodno realizovanih MAC procesora iste namene. Novi digitalni baseband procesor je prvi procesor te namene koji koristi diverziti-tehnike kombinovanja signala u okviru IEEE 802.11a komunikacionog standarda.

Radovi **e.4**, **e.5** i **g.17** prezentiraju rezultate implementacije, integracije i verifikacije RF-MIMO WLAN sistema veoma visoke pouzdanosti. Detaljno je opisana hardverska realizacija integrisanih kola RF frontend-a predajnika i prijemnika (BiCMOS ASIC), digitalnog baseband-a (FPGA) i MAC protokola (ASIC i FPGA). Integrisana kola analognog frontend-a koherentno kombinuju signale više predajnih i prijemnih antena u cilju postizanja bržeg i pouzdanijeg protoka podataka. Svakako, najveći naučni doprinos predstavlja značajno smanjenje složenosti hardvera i potrošnje energije uz očuvanje kvaliteta i reproduktivnosti signala. U skladu sa zahtevima novog RF frontend-a, projektovan je set ortogonalnih multi-band antena čime je obezbeđen polarizacioni diverzitet. Baseband PCB sadrži, pored FPGA baseband procesora, A/D i D/A konvertore i interfejse ka RF frontend PCB-u i MAC PCB-u. Takođe, implementiran je interfejs za vizuelno prikazivanje OFDM konstelacionih dijagrama i tri porta opšte namene za debagiranje. MAC PCB u formi CardBus modula integriše MIPS32 processor (ASIC u IHP 0.25 μm CMOS tehnologiji) sa 16-bitnim paralelnim baseband portom i hardver akceleratorom (FPGA Xilinx). Pored toga, razvijeni su softverski drajveri za Linux i Windows koji omogućavaju integraciju novog modema sa personalnim računarom. Kompletan RF-MIMO WLAN modem je prilagođen formi laptop računara i testiran u realnim uslovima. Rezultati testiranja verifikuju očekivana poboljšanja u odnosu na standardni IEEE 802.11a SISO sistem u pogledu tehničkih parametara (frame error rate) i korisničkih aplikacija (video stream transmission).

Rad **g.1** predstavlja novu arhitekturu IEEE 802.11 MAC protokola i njenu integraciju na čipu. Predložena arhitektura je realizovana u hardver-softver tehnici koja podrazumeva implementiranje kritičnih funkcija MAC protokola u hardveru. Ostale funkcije se izvršavaju u softveru na procesoru opšte namene. Opisan je kompletan ciklus projektovanja i realizacije sistema na čipu, počevši od specifikacije sistema, preko HDL modela za simulaciju i logičku sintezu, do layout-a i testiranja. Posebno treba istaći da je predloženi pristup i realizovani MAC sistem na čipu jedan od prvih te vrste.

Rad **g.22** prezentira rezultate istraživanja u oblasti komunikacionih sistema za asistenciju u vožnji. Opisan je prototip sistema na čipu koji omogućava video komunikaciju unutar dugih vozila (kamioni, autobusi i terenska vozila). Sistem je sposoban da šalje video signal u kabinu vozača bežičnim putem uz vrlo malo kašnjenje i veliku pouzdanost. Malo kašnjenje i veliku pouzdanost signala obezbeđuje video enkoder čije je vreme kodiranja i dekodiranja manje od 10 ms. Prvi rezultati testiranja pokazuju da je ukupno vreme obrade i slanja video signala od kamere do displeja u kabini vozača manje od 40 ms.

2.3. Učešće u međunarodnim i nacionalnim projektima

Kandidat je učestvovao u realizaciji tri naučno-istraživačka projekta koje je finansirala Republika Srbija:

- ***Razvoj tehnologija proizvodnje i projektovanja mikroelektronskih komponenata***, Elektronski fakultet, Niš, 1991-1995.
- ***Mikroelektronika i optoelektronika***, Elektronski fakultet, Niš, 1991-2000.
- ***Poluprovodnički senzori i dozimetri zračenja***, Elektronski fakultet, Niš, 1995-1996.

Učestvovao je i koordinirao rad projekta iz Programa FP7 Evropske unije:

- ***MIMAX – Advanced MIMO Systems for Maximum Reliability and Performance***, http://www.ict-mimax.eu, IHP, Frankfurt na Odri, 2008-2010.

Takođe je učestvovao u međunarodnom DAAD projektu:

- ***Embedded System Design***, http://systems.ihp-microelectronics.com/web/index.php5?id=48, BTU-Cottbus, 2009-2011.

Učesnik je i koordinator sledećih nacionalnih projekata:

- ***Modular Processor Library***, http://www.ihp-ffo.de/en/research/wireless-systems-and-applications/projects/mpl.html, IHP, Frankfurt na Odri, 2001-….
- ***Rear View Camera***, http://www.ihp-ffo.de/en/research/wireless-systems-and-applications/projects/rueckfahrkamera.html, IHP, Frankfurt na Odri, 2011-2012.

2.4. Nastavno-pedagoški rad

Kandidat dr Zoran Stamenković je stekao značajno nastavno-pedagoško iskustvo radeći kao vanredni profesor Elektronskog fakulteta u Nišu i saradnik Katedre za tehničku informatiku Brandenburškog tehničkog univerziteta u Cottbus-u. Osim toga, on je održao niz predavanja za mlade istraživače i studente-postdiplomce na Elektronskom fakultetu u Nišu, Elektrotehničkom fakultetu u Skoplju i Tehničkom fakultetu u Čačku:

- **Z. Stamenković**, “SOC Design at a Glance”, Lectures taught under auspice of the WUS Austria, Brain Gain Program, University of Niš, Faculty of Electronic Engineering, Niš (Serbia), December 13-24, 2004.

- **Z. Stamenković**, “SOC Design for Wireless Communications”, Lectures taught under auspice of the WUS Austria, Brain Gain Program, University of Niš, Faculty of Electronic Engineering, Niš (Serbia), January 30 - February 3, 2006.
- **Z. Stamenković**, “Configurable Processors”, Lectures taught under auspice of the WUS Austria, Brain Gain Program, University of Niš, Faculty of Electronic Engineering, Niš (Serbia), January 22-26, 2007.
- **Z. Stamenković**, “SOC Design: From System to Transistor”, DAAD Workshop on Embedded System Design, University of Niš, Faculty of Electronic Engineering, Niš (Serbia), June 29 - July 3, 2009, http://es.elfak.ni.ac.rs/Papers/Agenda_Nis_29Jun_3Jul_2009.pdf
- **Z. Stamenković**, “SOC Design for Wireless Sensor Networks”, DAAD Workshop on Embedded System Design, University Ss. Cyril and Methodius, Faculty of Electrical Engineering and Information Technologies, Skopje (Macedonia), October 26-28, 2009, http://systems.ihp-microelectronics.com/uploads/downloads/DAAD_Agenda_Skopje.pdf
- **Z. Stamenković**, “Advanced MIMO Systems for Maximum Reliability and Performance”, DAAD Workshop on Embedded System Design, University Ss. Cyril and Methodius, Faculty of Electrical Engineering and Information Technologies, Skopje (Macedonia), October 26-28, 2009, http://systems.ihp-microelectronics.com/uploads/downloads/DAAD_Agenda_Skopje.pdf
- **Z. Stamenković**, “SOC Design for Wireless Communications”, Lectures taught under auspice of the WUS Austria, Brain Gain Program, University of Kragujevac, Technical Faculty Čačak, Čačak (Serbia), May 10-14, 2010. - http://www.wus-austria.org/files/docs/Final%20Report%20Serbia.pdf
- **Z. Stamenković**, “Baseband and MAC Processors for RF-MIMO WLAN”, DAAD Workshop on Embedded System Design, University of Niš, Faculty of Electronic Engineering, Niš (Serbia), July 5-9, 2010, http://systems.ihp-microelectronics.com/uploads/downloads/DAAD2010_M2_Agenda.pdf
- **Z. Stamenković**, “Configurable Processors”, DAAD Workshop on Embedded System Design, University Ss. Cyril and Methodius, Faculty of Electrical Engineering and Information Technologies, Skopje (Macedonia), July 4-8, 2011, http://www.feit.ukim.edu.mk/fajlovi_pocetna/Agenda_Skopje_4_8_July_2011_final.pdf

2.5. Uredнички rad

Kandidat je pomoćnik urednika (Associate Editor) međunarodnog naučnog časopisa “Journal of Circuits, Systems, and Computers”, World Scientific Publishing Company, http://www.worldscinet.com/jcsc/mkt/editorial.shtml

2.6. Recenzentski rad

Kandidat je recenzent sledećih naučnih časopisa:

- IEEE Trans. on Semiconductor Manufacturing,
- IEEE Trans. on Vehicular Technology, http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6151269
- IEEE Design & Test of Computers,
- Microelectronics Reliability,

- International Journal of Electronics,

i sledećih naučnih skupova:

- Design Automation Conference (DAC),
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1688747
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4261128
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4555768
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5227217
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5523202
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5981912
  http://www.dac.com/external+reviewers.aspx
- IASTED International Conference on Circuits and Systems (CS),
- International Conference on Microelectronics (MIEL),
- IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5548594
- IEEE International Symposium on Circuits and Systems (ISCAS),
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4252541
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4541332
  http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5537173

2.7. Učešće u odborima naučnih skupova

Dr Zoran Stamenković je član programskog odbora sledećih naučnih skupova:

- IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems,
  http://iele.polsl.pl/ddecs2007/index.php?linkname=committees
  http://ui.sav.sk/DDECS2008/commitees.php?item=1
  http://ddecs2009.tul.cz/commitees.php?item=1
  http://ddecs2010.ecs.tuwien.ac.at/index.php?id=3
  http://ddecs2011.informatik.tu-cottbus.de/index.php?Id=commitee
  http://ddecs2012.ati.ttu.ee/index.php?page=8
- IASTED International Conference on Circuits and Systems,
  http://www.iasted.org/conferences/ipc-625.html
  http://www.iasted.org/conferences/ipc-712.html

2.8. Citiranost radova

S. Dimitrijev, N. Stojadinovic, and Z. Stamenkovic, "Yield Model for In-Line Integrated Circuit Production Control", *Solid-State Electronics*, vol. 31, pp. 975-979, 1988.

1. D. Dance and R. Jarvis, "Using Yield Models to Accelerate Learning Curve Progress", ***Proc. IEEE/SEMI International Semiconductor Manufacturing Science Symposium***, Burlingame (USA) 1990, (pp. 63-67), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=66108

2. A. Tyagi and M. Bayoumi, "Yield Modeling for Fault Tolerant WSI Arrays", ***Proc. IEEE International Symposium on Circuits and Systems***, New Orleans (USA) 1990, (pp. 1616-1619), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=112446

3. A. V. S. Satya, “Yield Measurement Tests Sites”, ***Proc. International Conference on Microelectronic Test Structures***, Kyoto (Japan) 1991, (pp. 141-144), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=161728
4. D. Dance and R. Jarvis, “Using Yield Models to Accelerate Learning Curve Progress”, ***IEEE Trans. Semiconductor Manufacturing***, vol. 5, pp. 41-46, 1992, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=121975

5. D. Dance and K. Gildersleeve, “Estimating Semiconductor Yield from Equipment Particle Measurements”, ***Proc. IEEE/SEMI International Semiconductor Manufacturing Science Symposium***, San Francisco (USA) 1992, (pp. 18-23), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=197629

6. D. Dance and R. Jarvis, “Application of Yield Models for Semiconductor Yield Improvement”, ***Proc. IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems***, Dallas (USA) 1992, (pp. 257-266), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=224349

7. A. H. Landzberg, ***Microelectronics Manufacturing Diagnostics Handbook***, Van Nostrand Reinhold, New York 1992, http://www.amazon.com/Microelectronics-Manufacturing-Diagnostics-Electrical-Engineering/dp/0442004710

8. G. K. Rao, ***Multilevel Interconnect Technology***, McGraw-Hill, New York 1993, http://www.amazon.com/Multilevel-Interconnect-Technology-Intel-Mcgraw-Hill/dp/0070512248

9. S. P. Cunningham, “The Development and Use of In-line Yield Estimates in Semiconductor Manufacturing”, University of California at Berkeley, ***Ph.D. Thesis***, 1995, http://bcam.berkeley.edu/ARCHIVE/theses/scunning.PhD.pdf

10. M. G. Pecht, R. Radojcic, and G. K. Rao, ***Guidebook for Managing Silicon Chip Reliability***, CRC Press, Boca Raton 1998, http://www.crcpress.com/shopping_cart/products/product_detail.asp?sku=9624&af=W1129

11. A. A. Nazarov, ***Design of test structures for evaluation of VLSIC technologies***, ***Ph.D. Thesis***, 2000, http://www.dissercat.com/content/proektirovanie-testovykh-skhem-dlya-attestatsii-tekhnologicheskikh-protsessov-proizvodstva-s

Z. Stamenkovic and N. Stojadinovic, “Chip Yield Modeling Related to Photolithographic Defects”, *Microelectronics and Reliability*, vol. 32, pp. 663-668, 1992.

1. F. Corsi, S. Martino, C. Marzocca, R. Tangorra, C. Baroni, and M. Buraschi, “Critical Areas for Finite Length Conductors”, ***Microelectronics and Reliability***, vol. 32, pp. 1539-1544, 1992, http://dx.doi.org/10.1016/0026-2714(92)90453-R

2. K. O. Kim, “Relating Integrated Circuit Yield and Time-Dependent Reliability for Various Defect Density Distributions”, ***IEEE Trans. Reliability***, vol. 55, pp. 307-313, 2006, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=1638413

3. W. Kuo, K. Kim, and T. Kim, "Modeling and Analyzing Yield, Burn-In and Reliability for Semiconductor Manufacturing: Overview" in ***Springer Handbook of Engineering Statistics (Editor Hoang Pham)***, Springer London, pp. 153-169, 2006, http://www.springerlink.com/content/w147812324n81473/

Z. Stamenkovic and N. Stojadinovic, "New Defect Size Distribution Function for Estimation of Chip Critical Area in Integrated Circuit Yield Models", *Electronics Letters*, vol. 28, pp. 528-530, 1992.

1. F. Corsi, S. Martino, C. Marzocca, R. Tangorra, C. Baroni, and M. Buraschi, "Critical Areas for Finite Length Conductors", ***Microelectronics and Reliability***, vol. 32, pp. 1539-1544, 1992, http://dx.doi.org/10.1016/0026-2714(92)90453-R

2. R. D. Nelson and E. M. Witteles, "Large Area Image Plane Sensors for Radiography", ***Journal of X-Ray Science and Technology***, vol. 4, pp. 353-360, 1994, http://linkinghub.elsevier.com/retrieve/pii/S0895399605800527

3. C. H. Stapper and R. J. Rosner, "Integrated Circuit Yield Management and Yield Analysis: Development and Implementation", ***IEEE Trans. Semiconductor Manufacturing***, vol. 8, pp. 95-102, 1995, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=388016

4. G. A. Allan and A. J. Walton, "Efficient Critical Area Measurements of IC Layout Applied to Quality and Reliability Enhancement", ***Microelectronics and Reliability***, vol. 37, pp. 1825-1833, 1997, http://dx.doi.org/10.1016/S0026-2714(97)00021-8

5. K. Nakamae, H. Ohmori, and H. Fujioka, "A Simple VLSI Spherical Particle-Induced Yield Predictor", ***Proc. International Conference on Modeling and Simulation of Microsystems***, San Juan (USA) 1999, (pp. 479-482), http://www.comppub.com/publications/MSM/99/pdf/T5301.pdf

6. W. Kuo and T. Kim, "An Overview of Manufacturing Yield and Reliability Modeling for Semiconductor Products", ***Proceedings of the IEEE***, vol. 87, pp. 1329-1344, 1999, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=775417

7. W. Kuo and T. Kim, "Semiconductor Device Manufacture Yield and Reliability Modeling", ***Wiley Encyclopedia of Electrical and Electronics Engineering***, 1999, http://onlinelibrary.wiley.com/doi/10.1002/047134608X.W7045/abstract

8. K. Nakamae, H. Ohmori, and H. Fujioka, "A Simple VLSI Spherical Particle-Induced Fault Simulator: Application to DRAM Production Process", ***Microelectronics Reliability***, vol. 40, pp. 245-253, 2000, http://dx.doi.org/10.1016/S0026-2714(99)00228-0

9. X. Xuan, A. D. Singh, and A. Chatterjee, "Reliability Evaluation for Integrated Circuit with Defective Interconnect under Electromigration", ***Proc. 4th IEEE International Symposium on Quality Electronic Design***, San Jose (USA) 2003, (pp. 29-34), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=1194705

10. X. Xuan, “Analysis and Design of Reliable Mixed-Signal CMOS Circuits”, Georgia Institute of Technology, School of Electrical and Computer Engineering, ***Ph.D. Thesis***, 2004, http://etd.gatech.edu/theses/available/etd-08032004-185515/unrestricted/xuan_xiangdong_200412_phd.pdf

11. K. O. Kim, “Relating Integrated Circuit Yield and Time-Dependent Reliability for Various Defect Density Distributions”, ***IEEE Trans. Reliability***, vol. 55, pp. 307-313, 2006, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=1638413

12. X. Xuan, A. D. Singh, and A. Chatterjee, “Lifetime Prediction and Design-for-Reliability of IC Interconnections with Electromigration Induced Degradation in the Presence of Manufacturing Defects”, ***Journal of Electronic Testing***, vol. 22, pp. 471-482, 2006, http://www.springerlink.com/content/31p2286457363097/

13. W. Kuo, K. Kim, and T. Kim, “Modeling and Analyzing Yield, Burn-In and Reliability for Semiconductor Manufacturing: Overview” in ***Springer Handbook of Engineering Statistics (Editor Hoang Pham)***, Springer London, pp. 153-169, 2006, http://www.springerlink.com/content/w147812324n81473/

14. M. Sachdev and J. P. de Gyvez, ***Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits: Functional and Parametric Defect Models***, Springer US, pp. 23-67, 2007, http://www.springerlink.com/content/u542483j1561t531/

15. M. Sachdev and J. P. de Gyvez, ***Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits: Yield Engineering***, Springer US, pp. 289-315, 2007, http://www.springerlink.com/content/g43202r649364466/

16. K. O. Kim and H.-S. Oh, “Reliability Functions Estimated from Commonly Used Yield Models”, ***Microelectronics Reliability***, vol. 48, pp. 481-489, 2008, http://dx.doi.org/10.1016/j.microrel.2007.08.001

Z. Stamenkovic, “Algorithm for Extracting Integrated Circuit Critical Areas Associated with Point Defects”, *International Journal of Electronics*, vol. 77, pp. 369-376, 1994.

1. G. A. Allan and A. J. Walton, “Efficient Critical Area Measurements of IC Layout Applied to Quality and Reliability Enhancement”, ***Microelectronics and Reliability***, vol. 37, pp. 1825-1833, 1997, http://dx.doi.org/10.1016/S0026-2714(97)00021-8

2. J. P. de Gyvez, “Yield Modeling and BEOL Fundamentals”, ***Proc. International Workshop on System-Level Interconnect Prediction***, Sonoma (USA) 2001, (pp. 135-163), http://dl.acm.org/citation.cfm?id=368821&dl=ACM&coll=DL&CFID=75900759&CFTOKEN=84415792

Z. Stamenkovic and S. Mitrovic, “Integrated Circuit Yield Prediction”, *Proc. 20th International Conference on Microelectronics*, Nis (Serbia) 1995, (pp. 479-483)

1. Y. Nakamura, J. Savir, and H. Fujiwara, “Effect of BIST Pretest on IC Defect Level”, ***IEICE Transactions on Information and Systems***, vol. E89-D, pp. 2626-2636, 2006, http://dx.doi.org/10.1093/ietisy/e89-d.10.2626

2. Y. Nakamura, “Studies on Defect Level and Diagnosis for Built-in Self Test Architecture”, Nara Institute of Science and Technology, Department of Information Processing, ***Ph.D. Thesis***, 2006, http://library.naist.jp/mylimedio/dllimedio/show.cgi?bookid=89548

Z. Stamenkovic, N. Stojadinovic, and S. Dimitrijev, “Modeling of Integrated Circuit Yield Loss Mechanisms”, *IEEE Trans. Semiconductor Manufacturing*, vol. 9, pp. 270-272, 1996.

1. R. E. Bohn and C. Terwiesch, “The Economics of Yield-Driven Processes”, ***Technical Report***, University of California, Information Storage Industry Center, pp. 1-32, 1997, http://repositories.cdlib.org/cgi/viewcontent.cgi?article=1012&context=isic

2. R. E. Bohn and C. Terwiesch, “The Economics of Yield-Driven Processes”, ***Journal of Operations Management***, vol. 18, pp. 41-59, 1999, http://dx.doi.org/10.1016/S0272-6963(99)00014-5

3. P. Miskowiec, “Layout and Defect Related Yield and Lifetime Modeling of Microelectronic Circuits”, University of Duisburg, Department of Electrical Engineering, ***Ph.D. Thesis***, 2000, http://www.ub.uni-duisburg.de/diss/diss0031/9.pdf

4. L. Ludwig, E. Sapozhnikova, V. Lunin, and W. Rosenstiel, “Error Classification and Yield Prediction of Chips in Semiconductor Industry Applications”, ***Neural Computing & Applications***, vol. 9, pp. 202-210, 2000, http://springerlink.metapress.com/app/home/contribution.asp?wasp=92xd8tgbwp6qrn9e5ee7&referrer=parent&backto=searcharticlesresults,1,1;journal,1,1;browsepublicationsresults,391,543

5. Masaaki Sugimoto, “Inspection and Analyzing Apparatus for Semiconductor Integrated Circuit”, ***United States Patent 6374199***, 2002, http://www.patentstorm.us/patents/6374199-fulltext.html

6. F. L. Chen, Sheng-Che Lin, K. Yih-Yuh Doong, and K. L. Young, “LOGIC Product Yield Analysis by Wafer Bin Map Pattern Recognition Supervised Neural Network”, ***Proc. IEEE International Symposium on Semiconductor Manufacturing***, San Jose (USA) 2003, (pp. 501-504), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=1243336

7. C.-H. Liao, “Development of Yield Prediction Model for Wafer-Cutting Process Taking into Account Process Type and Volume”, National Cheng Kung University, Department of Industrial and Information Management, ***Master’s Thesis***, 2005, http://etdncku.lib.ncku.edu.tw/ETD-db/ETD-search/getfile?URN=etd-0826105-045937&filename=etd-0826105-045937.pdf

8. Y. Nakamura, J. Savir, and H. Fujiwara, “Defect Level vs. Yield and Fault Coverage in the Presence of an Unreliable BIST”, ***IEICE Transactions on Information and Systems***, vol. E88-D, pp. 1210-1216, 2005, http://dx.doi.org/10.1093/ietisy/e88-d.6.1210

9. L.-J. Wei, “Development of Wafer Bin Map Pattern Recognition Model Using Neural Network Approach”, Tsinghua University, Industrial Engineering and Engineering Management, ***Master’s Thesis***, 2006, http://nthur.lib.nthu.edu.tw/handle/987654321/35446

10. Y. Nakamura, J. Savir, and H. Fujiwara, “Effect of BIST Pretest on IC Defect Level”, ***IEICE Transactions on Information and Systems***, vol. E89-D, pp. 2626-2636, 2006, http://dx.doi.org/10.1093/ietisy/e89-d.10.2626

11. Y. Nakamura, “Studies on Defect Level and Diagnosis for Built-in Self Test Architecture”, Nara Institute of Science and Technology, Department of Information Processing, ***Ph.D. Thesis***, 2006, http://library.naist.jp/mylimedio/dllimedio/show.cgi?bookid=89548

12. J. C. Ho, “Technology evaluation in Taiwan's technology industries: Strategies, trajectories, and innovations”, ***Technological Forecasting and Social Change***, vol. 78, pp. 1379-1388, 2011, http://www.sciencedirect.com/science/article/pii/S004016251100059X

Z. Stamenkovic, H.-Ch. Dahmen, and U. Glaeser, “Model Evaluation Using Genetic Manipulation Techniques”, *Proc. 9th Great Lakes Symposium on VLSI*, Ann Arbor (USA) 1999, (pp. 224-225)

1. J. T. Alander, “An Indexed Bibliography of Genetic Algorithms and Computer Aided Design”, University of Vaasa, Dept of Electrical Engineering and Production Economics, ***Report Series No. 94-1-CAD***, 2003, ftp://ftp.uwasa.fi/cs/report94-1/gaCADbib.ps.Z

Z. Stamenkovic, H.-Ch. Dahmen, and U. Glaeser, “VHDL Design Validation by Genetic Manipulation Techniques”, *Proc. 22nd International Conference on Microelectronics*, Nis (Serbia) 2000, (pp. 735-738)

1. G. Rolland and R. Desplats, “Method for Locating Faulty Elements in an Integrated Circuit”, ***United States Patent 6526546***, 2003, http://www.patentstorm.us/patents/6526546-fulltext.html

2. C. Luo, J. Yang, and M. Ling, “Coverage Directed Vector Generation for Functional Verification Using Genetic Algorithm”, ***Journal of Applied Sciences (Chinese)***, vol. 23, pp. 375-379, 2005, http://d.wanfangdata.com.cn/Periodical_yykxxb200504010.aspx

3. D. K. Pradhan and I. G. Harris, ***Practical Design Verification***, Cambridge University Press, 2009, http://81.70.242.211/eab/manual/Publisher/Cambridge%20University%20Press%20www.cambridge.org/practical%20design%20verification%209780521859721%2052137%20c20100215%20%5B290%5D.pdf

4. A. Cheng, “Verification of System-on-Chips Using Genetic Evolutionary Test Techniques from a Software Applications Perspective”, University of Adelaide,

School of Electrical and Electronic Engineering, ***Ph.D. Thesis***, 2009, http://digital.library.adelaide.edu.au/dspace/bitstream/2440/62335/2/02main.pdf

Z. Stamenkovic, "Testing and Yield of Integrated Circuits", *Proc. 4th IEEE International Symposium on Quality Electronic Design (Tutorial: Track B)*, San Jose (USA) 2003.

1. Duane Boning, "**Control of Manufacturing Processes: Yield Modeling**", Massachusetts Institute of Technology, ***Lecture***, March 2008, http://ocw.mit.edu/courses/mechanical-engineering/2-830j-control-of-manufacturing-processes-sma-6303-spring-2008/video-lectures/lecture10.pdf

Z. Stamenkovic, M. Giles, and F. Russi, "Combining Internal Scan Chains and Boundary Scan Register: A Case Study", *Proc. IEEE Region 8 EUROCON 2009 Conference*, Saint-Petersburg (Russia) 2009, (pp.2064-2069)

1. C.-Y. Chang, "Random Pattern Testing for MCM Interconnect Using Computer Generated Hologram Technology", ***Proc. 9th International Conference on Machine Learning and Cybernetics***, Qingdao (China) 2010, (pp. 2653-2657), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5580914

2. F. G. Zadegan, "Analysis and Optimization for Testing Using IEEE P1687", Linköpings University, Department of Computer and Information Science, ***Master's Thesis***, 2010, http://liu.diva-portal.org/smash/record.jsf?searchId=1&pid=diva2:357396

3. F. G. Zadegan, U. Ingelsson, G. Carlsson, and E. Larsson, "Access Time Analysis for IEEE P1687", ***IEEE Trans. on Computers***, 2011, http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=5999657

G. Panic, D. Dietterle, Z. Stamenkovic, and K. Tittelbach-Helmrich, "A System-on-Chip Implementation of the IEEE 802.11a MAC Layer", *Proc. 6th IEEE EUROMICRO Symposium on Digital System Design*, Antalya (Turkey) 2003, (pp. 319-324)

1. A. Jiang, F. Ren, G. Li, Y. Pang, T. Ban, W. Gou, X. Wang, X. Wu, H. Chen, and G. Zhang, "The Design of an IEEE802.11 WLAN Hardware MAC", ***Proc. 7th International Conference on Solid-State and Integrated Circuits Technology***, Beijing (China) 2004, (pp. 1380-1383), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=1436814

2. S. Lee, S. Jin, Y. Kim, and K. Cho, "An Architecture for Wireless LAN/MAN Packet Processor", ***Proc. 60th IEEE Vehicular Technology Conference***, Los Angeles (USA) 2004, (pp. 3206-3209), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=1404653

3. I.-G. Lee, S.-B. Lee, and S.-C. Park, "Effective Co-Verification of IEEE 802.11a MAC/PHY Combining Emulation and Simulation Technology", ***Proc. 38th IEEE Annual Simulation Symposium***, San Diego (USA) 2005, (pp. 138-146), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=1401960

4. A. Hussain, X.-Z. Lou, W. Zhong, and Z.-G. Mao, "A Study on IEEE 802.11 WLAN Implementation with Embedded Microprocessor", ***Journal of Harbin Institute of Technology (Chinese)***, vol. 12, pp. 365-369, 2005, http://d.wanfangdata.com.cn/Periodical_hebgydxxb-e200504003.aspx

5. C.-H. Weng, "FPGA Implementation of 802.11b MAC Controller: Transmitter", Tatung University, Department of Electrical Engineering, ***Master's Thesis***, 2005, http://ethesys.library.ttu.edu.tw/ETD-db/ETD-search/view_etd?URN=etd-1229105-133722

6. C.-F. Wu, "FPGA Implementation of IEEE 802.11b/g Mixed-Mode MAC Controller", Institute of Communications Engineering, ***Master's Thesis***, 2005, http://ethesys.library.ttu.edu.tw/ETD-db/ETD-search-c/view_etd?URN=etd-0829105-154304

7. H.-W. Chen, "Behavioral Modeling of IEEE 802.11e Media Access Control Chip with Cross-Layer Interface Using Specification and Description Language", Kun Shan University, Department of Electronic Engineering, ***Master's Thesis***, 2005, http://www.cetd.com.cn/ec/thesisDetail.aspx?etdun=U0025-0306200810420090

8. Yu-Yi Chao, "Design and FPGA Implementation of an Energy-Efficient Architecture for the Medium Access Controller of IEEE 802.11 WLANs", Chung Hua University, Department of Electrical Engineering, ***Master's Thesis***, 2006 http://ndltd.ncl.edu.tw/cgi-bin/gs32/gsweb.cgi/login?o=dnclcdr&s=id=%22094CHPI0442009%22.&searchmode=basic

9. T. Ban, X.-F. Gu, A.-P. Jiang, G.-X. Zhang, and X.-A. Wang, "An IEEE802.11-Based SoftMAC Implementation Method", ***Microelectronics & Computer (Chinese)***, vol. 23, pp. 4-7, 2006, http://www.ceps.com.tw/ec/ecjnlarticleView.aspx?atliid=258479&issueiid=22429&jnliid=2387

10. S. Samadi, A. Golmohammadi, A. Jannesari, M.R. Movahedi, B. Khalaj, and S. Ghaemmaghami, "A Novel Implementation of the IEEE802.11 Medium Access Control", ***Proc. International Symposium on Intelligent Signal Processing and Communication Systems***, Tottori (Japan) 2006, (pp. 489-492), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4212322

11. X. Wanang, F. Zhi, and S. Yin, "The Design and Implementation of the IEEE 802.11 MAC Based on Soft-Core Processor and RTOS", ***Journal of Electronics (Chinese)***, vol. 24, pp. 232-237, 2007, http://www.springerlink.com/content/561818325wkk6372/

12. H. Hinkelmann, P. Zipf, M. Glesner, and T. Pionteck, "Dynamically Reconfigurable Computing for Wireless Communication Systems", ***Information Technology***, vol. 49, pp. 174-180, 2007, http://www.atypon-link.com/OLD/doi/pdf/10.1524/itit.2007.49.3.174

13. S. W. Nabi, C. C. Wells, and W. Vanderbauwhede, "A Dynamically Reconfigurable System-on-Chip for Implementing Wireless MACs", ***Proc. 3rd IEEE Ph.D. Research in Microelectronics and Electronics Conference***, Bordeaux (France) 2007, (pp. 37-

40),
http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?tp=&arnumber=4401805&isnumber=4401782

14. S. W. Nabi, C. C. Wells, and W. Vanderbauwhede, "Towards a Reconfigurable SoC for Wireless MACs in Consumer Handheld Devices", ***Proc. the First International Conference on Computer, Control, and Communication***, Karachi (Pakistan) 2007, (pp. 39-48), http://www.ic-4.org/proceeding/p39.pdf

15. C.-L. Chen et al., "Analysis and Realization of IEEE 802.11e Medium Access Control Quality of Service Enhancement by Using Fuzzy Feedback Control Model", Kun Shan University, Department of Electronic Engineering, ***Tech. Report***, October 2007, pp. 1-72,
http://ir.lib.ksu.edu.tw:8080/dspace/bitstream/987654321/6385/1/952221E168029.pdf

16. C.-L. Chen, "Morphisms from IEEE 802.11 DCF Specifications to its EDCA QoS Practice with Cross-Layer Interface", ***Proc. International Conference on Parallel and Distributed Systems***, Hsinchu (Taiwan) 2007, (vol. 2, pp. 1-8),
http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4447790

17. D. Dietterle, "Hardware-Protokollbeschleuniger für eine Verbindungssicherungs-Protokollebene eines Senderempfängers", ***German Patent 102007003634B3***, 2008,
http://www.patent-de.com/20080424/DE102007003634B3.html

18. C. Sauer, M. Gries, and H.-P. Löb, "SystemClick - A Domain-Specific Framework for Early Exploration Using Functional Performance Models", ***Proc. 45th ACM/IEEE Design Automation Conference***, Anaheim (USA) 2008, (pp. 480-485),
http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4555865

19. S. W. Nabi, C. C. Wells, and W. Vanderbauwhede, "A Dynamically Reconfigurable Hardware Co-Processor for a Multi-Standard Wireless MAC Processor", ***Proc. 3rd NASA/ESA Conference on Adaptive Hardware and Systems***, Noordwijk (Netherlands) 2008, (pp. 368-375),
http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4584296

20. S. W. Nabi, C. C. Wells, and W. Vanderbauwhede, "Interface and Reconfiguration Controller for a Wireless MAC-Oriented Dynamically Reconfigurable Hardware Co-Processor", ***Proc. 18th International Conference on Field Programmable Logic and Applications***, Heidelberg (Germany) 2008, (pp. 591-594),
http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4630016

21. S. W. Nabi, "A Coarse-Grained Dynamically Reconfigurable MAC Processor for Power-Sensitive Multi-Standard Devices", Institute for System Level Integration Livingston, ***Ph.D. Thesis***, 2008, http://theses.gla.ac.uk/865/01/2009nabiengd.pdf

22. R. Eickhoff, R. Kraemer, I. Santamaria, L. Gonzalez, P. Sperandio, and H. Neophytou, "Integrated Low Power RF-MIMO Transceiver for Enhanced 802.11a Short Range Communication", ***Proc. 21st Wireless World Research Forum Meeting***, Stockholm (Sweden) 2008, http://www.wireless-world-research.org/fileadmin/sites/default/files/meetings/Past%20Meetings/2008/WWRF21/Presentations%20and%20Papers/WG5/papers/Integrated_low_power_RF-MIMO_transceiver_for_enhanced_802.11a_short_range_communication.pdf

23. B. Kim, Y. Kim, D. Lee, and S. Tak, “A Reconfigurable NoC Platform Incorporating Real-Time Task Management Technique for H/W-S/W Codesign of Network Protocols”, ***Proc. International Symposium on Ubiquitous Multimedia Computing***, Hobart (Australia) 2008, (pp. 238-243), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4656552

24. Y. Kim, H. Lee, and J. Kim, “Cross-Layer Optimization Based 802.11e MAC Processor Toward Wireless Body Area Network”, ***Proc. 3rd International Conference on Convergence and Hybrid Information Technology***, Busan (Korea) 2008, (pp. 33-37), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4682209

25. H.-P. Löb, M. Gries, and C. Sauer, “Implementing a Software-Based 802.11 MAC on a Customized Platform”, ***Proc. 6th Annual IEEE Consumer Communications and Networking Conference***, Las Vegas (USA) 2009, (pp. 677-682), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4784695

26. R. Eickhoff, R. Kraemer, I. Santamaria, and L. Gonzalez, “Developing energy-efficient MIMO radios”, ***IEEE Vehicular Technology Magazine***, vol. 4, pp. 34-41, 2009, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4906421

27. Y. Kim, E. K. Park, and S. Tak, “Dynamically Reconfigurable Hardware–Software Architecture for Partitioning Networking Functions on the SoC Platform”, ***Journal of Systems and Software***, vol. 82, pp. 1588-1599, 2009, http://dx.doi.org/10.1016/j.jss.2009.03.015

28. . Y.-G. Lee and Y.-J. Jeong, “Design and Implementation of MAC Engine for Next-Generation WLAN”, ***Journal of the Institute of Elect. Engineers of Korea (Semiconductor and Devices)***, vol. 46, pp. 39-47, 2009, http://www.koreascience.or.kr/article/articleresultdetail.jsp?no=49968653&searchtype=JSB&listlen=9&listno=6

29. Y. Kim, T. Kim, E. K. Park, and S. Tak, “A Novel Hardware-Software Codesign of Network Protocol Stacks on a SoC Platform”, ***Proc. 18th International Conference on Computer Communications and Networks***, San Francisco (USA) 2009, (pp. 1-6), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5235286

30. J. Gabarron, E. Lopez, and J. Haro, “Evaluacion de mecanismos de priorizacion en 802.11p con VHDL”, ***VII Jornadad de Ingenieria Telematica***, Cartagena (Spain) 2009, (pp. 190-196), http://ait.upct.es/~eegea/pub/jitel09-2.pdf

31. H.-P. Löb and C. Sauer, “A Modular Reference Application for IEEE 802.11n Wireless LAN MACs”, ***Proc. IEEE International Conference on Communications***, Dresden (Germany) 2009, (pp. 1-5), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5198631

32. H.-P. Löb, C. Liss, U. Ruckert, and C. Sauer, “UMAC - A Universal MAC Architecture for Heterogeneous Home Networks”, ***Proc. International Conference on Ultra Modern Telecommunications***, Sankt Petersburg (Russia) 2009, (pp. 1-6), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5345503

33. C. Sauer, “Application-driven Development of Flexible Packet-oriented Communication Interfaces”, Technical University Munich, Institute for Integrated

Systems, ***PhD Thesis***, 2010, http://deposit.d-nb.de/cgi-bin/dokserv?idn=1007539259&dok_var=d1&dok_ext=pdf&filename=1007539259.pdf

34. M. L. Huang, J. Lee, H. Setiawan, H. Ochi, and S.-C. Park, "A High Throughput Medium Access Control Implementation Based on IEEE 802.11e Standard", ***IEICE Trans. on Communications***, vol. E93.B, pp. 948-960, 2010, http://dx.doi.org/10.1587/transcom.E93.B.948

Z. Stamenkovic, C. Wolf, G. Schoof, and J. Gaisler, "LEON-2: General Purpose Processor for a Wireless Engine", *Proc. 9th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems,* Prague (Czech Republic) 2006, (pp. 50-53)

1. M. Portolan, "Dependable and Secure Design of an Embedded System", Grenoble Institute of Technology, ***Ph.D. Thesis***, 2006, http://tel.archives-ouvertes.fr/docs/00/16/39/80/PDF/dsd_0251.pdf

2. R. Magness, "Short-range RF Wireless (Proximity) Networks Technology Assessment for Space Applications", European Space Agency, ***Tech. Note***, April 2006, pp. 1-105, http://emits.esa.int/emits-doc/1-5200-RD1-ESA-Wireless-Dossier-AnnexA-Draft-R0.pdf

3. W. C. Wilson, N. C. Coffey, and E. I. Madaras, "Leak Detection and Location Technology Assessment for Aerospace Applications", NASA Langley Research Center, ***Tech. Report***, Hampton (USA), September 2008, pp. 1-27, http://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20080041598_2008040602.pdf

4. P. Langendörfer, F. Vater, and K. Piotrowski, "Customizing Sensor Nodes and Software for Individual Pervasive Health Applications", ***Proc. 3rd International Conference on Pervasive Computing Technologies for Healthcare***, London (UK) 2009, (pp. 1-4), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5191158

5. T. Vladimirova and J. R. Paul, "Implementation of an IEEE802.11a Transmitter Module for a Reconfigurable System-on-a-Chip Design", ***Proc. 4th NASA/ESA Conference on Adaptive Hardware and Systems***, San Francisco (USA) 2009, (pp. 305-312), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5325440

6. G. V. Morozov and R. O. Maslennikov, "Development of a Custom Processor for Multi-protocol Wireless Communication System", ***Proc. 14th Scientific Conference on Radiophysics***, Nizhni Novgorod (Russia) 2010, (pp. 225-226), http://www.rf.unn.ru/rus/sci/books/10/pdf/bionics.pdf

7. L. Liang-Liang and J. Peng-Long, "The Design of PLC SOC Controller by Dual-Core Mutually Exclusive Processor", ***Proc. International Conference on Electrical Engineering and Automatic Control***, Zibo (China) 2010, (pp. 534-537), http://www.docin.com/p-160848841.html

8. L. Liang-Liang and J. Peng-Long, "The Design of PLC SOC Controller by Dual-Core Mutually Exclusive Processor", ***Advanced Materials Research***, vol. 383-390, pp. 5663-5668, 2012, http://www.scientific.net/AMR.383-390.5663

9. A. V. Mahatme and R. S. Pande, "Development of Design Environment for Embedded SOC Application", ***International Journal of Systems, Algorithms and Applications***, vol. 2, pp. 34-38, 2012, http://ijsaa.org/9ICTM110212.pdf

Z. Stamenkovic, C. Wolf, G. Schoof, and J. Gaisler, "An Implementation Study on Fault Tolerant LEON-3 Processor System", *Proc. 7th IP-Based System-on-Chip Design Conference*, Grenoble (France) 2006, (pp. 23-26)

1. P. Reyes, P. Reviriego, J. A. Maestro, and O. Ruano, "Fault Tolerance Analysis of Communication System Interleavers: the 802.11a Case Study", ***The Journal of Signal Processing Systems***, vol. 52, pp. 231-247, 2008, http://www.springerlink.com/content/f2h264780x505472/

2. W. C. Wilson, N. C. Coffey, and E. I. Madaras, "Leak Detection and Location Technology Assessment for Aerospace Applications", NASA Langley Research Center, ***Tech. Report***, Hampton (USA), September 2008, pp. 1-27, http://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20080041598_2008040602.pdf

Z. Stamenkovic, D. Dietterle, G. Panic, W. Bocer, G. Schoof, and J.-P. Ebert, "MAC Processor for BASUMA Wireless Body Area Network", *Proc. 5th IASTED International Conference on Circuits, Signals, and Systems*, Banff (Canada) 2007, (pp. 47-52)

1. D. Dietterle, "Embedded System Protocol Design Flow Based on SDL: From Specification to Hardware/Software Implementation", ***Proc. International Conference on Simulation Tools and Techniques for Communications, Networks and Systems***, Marseille (France) 2008, http://portal.acm.org/citation.cfm?id=1416222.1416289&coll=portal&dl=GUIDE

2. M. A. Ameen, A. Nessa, and K. S. Kwak, "QoS Issues with Focus on Wireless Body Area Networks", ***Proc. 3rd International Conference on Convergence and Hybrid Information Technology***, Busan (Korea) 2008, (pp. 801-807), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4682127

3. D. Dietterle, **"**Efficient Protocol Design Flow for Embedded Systems", Brandenburg University of Technology Cottbus, ***Ph.D. Thesis***, 2009, http://opus.kobv.de/btu/volltexte/2009/784/pdf/thesis_dietterle.pdf

4. D. Dietterle and R. Kraemer, "A Hardware Accelerated Implementation of the IEEE 802.15.3 MAC Protocol", ***Telecommunication Systems***, vol. 40, pp. 161-167, 2009, http://www.springerlink.com/content/lr57566h55342j17/

Z. Stamenkovic, G. Panic, and G. Schoof, "A System-On-Chip for Wireless Body Area Sensor Network Node", *Proc. 11th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems*, Bratislava (Slovakia) 2008, (pp.132-135)

1. D. Nunes, T.-D. Tran, D. Raposo, A. Pinto, A. Gomes, and J. S. Silva, "A Web Service-Based Framework Model for People-Centric Sensing Applications Applied to Social Networking", ***Sensors***, vol. 12, pp. 1688-1701, 2012, http://dx.doi.org/10.3390/s120201688

2. C. Ragit and S. Badjate, “Mixed Signal Interface Chip for Wearable Healthcare System”, ***International Journal of Computer Applications***, vol. NCIPET(7), pp. 15-18, 2012, http://www.ijcaonline.org/proceedings/ncipet/number7/5240-1052

G. Panic, Z. Stamenkovic, and R. Kraemer, “Power Gating in Wireless Sensor Networks”, *Proc. 3rd IEEE International Symposium on Wireless Pervasive Computing*, Santorini Island (Greece) 2008, (pp. 499-503)

1. K. Kawasaki, T. Shiota, K. Nakayama, and A. Inoue, “A Sub-µs Wake-Up Time Power Gating Technique with Bypass Power Line for Rush Current Support”, ***IEEE Journal of Solid-State Circuits***, vol. 44, pp. 1178-1183, 2009, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4804973

2. C. Lahuec, M. Arzel, M. Gouriou, and F. Gallee, “A Ligament Laxity Telemetry System Architecture for a Knee Replacement Prosthesis”, ***Proc. 2nd International Symposium on Applied Sciences in Biomedical and Communication Technologies***, Bratislava (Slovakia) 2009, (pp. 1-6), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5373664

3. A. Niedermeier, K. Svarstad, F. Bouwens, J. Hulzink, and J. Huisken, “The Challenges of Implementing Fine-Grained Power Gating”, ***Proc. 20th Great Lakes Symposium on VLSI***, Providence, Rhode Island (USA) 2010, (pp. 361-364), http://portal.acm.org/citation.cfm?id=1785564&dl=ACM&coll=ACM&CFID=89598046&CFTOKEN=28843286

4. A. Sathanur, M. Ashouei, and J. Huisken, “Improving Efficiency of Power Gated Circuits Through Concurrent Optimization of Power Switch Size and Forward Body Biasing”, ***Proc. IEEE International Conference on IC Design and Technology***, Grenoble (France) 2010, (pp. 178-181), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5510265

5. M. Enachescu, G. Voicu, and S. Dan Cotofana, “Advanced NEMS-Based Power Management for 3D Stacked Integrated Circuits”, ***Proc. International Conference on Energy Aware Computing***, Cairo (Egypt) 2010, (pp. 1-4), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5702286

6. A. Merentitis, N. Kranitis, A. Paschalis, and D. Gizopoulos, “Low Energy On-Line Self-Test of Embedded Processors in Dependable WSN Nodes”, ***IEEE Trans. Dependable and Secure Computing***, vol. 9, pp. 86-100, 2012, http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5714702

7. U. Alvarado, G. Bistue, and I. Adin, “Low Power RF Circuit Design in Standard CMOS Technology: Schematic Design Techniques for Power Saving in RF”, ***Springer Lecture Notes in Electrical Engineering***, vol. 104, pp. 61-85, 2012, http://www.springerlink.com/content/qw773v8218t4053x/

G. Panic, D. Dietterle, and Z. Stamenkovic, “Architecture of a Power-Gated Wireless Sensor Node”, *Proc. 11th IEEE EUROMICRO Conference on Digital System Design*, Parma (Italy) 2008, (pp. 844-849)

1. G. Panic, T. Basmer, K. Tittelbach-Helmrich, and L. Lopacinski, "Low Power Sensor Node Processor Architecture", ***17th IEEE International Conference on Electronics, Circuits, and Systems***, Athens (Greece) 2010, (pp. 914-917), http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=5724661
2. U. Alvarado, G. Bistue, and I. Adin, "Low Power RF Circuit Design in Standard CMOS Technology: Schematic Design Techniques for Power Saving in RF", ***Springer Lecture Notes in Electrical Engineering***, vol. 104, pp. 61-85, 2012, http://www.springerlink.com/content/qw773v8218t4053x/

M. Mitic, M. Stojcev, and Z. Stamenkovic, *Digital Systems and Applications: An Overview of SOC Buses* (edited by V. Oklobdzija), CRC Press, Boca Raton 2008.

1. M. A. Zabidi and M. N. Marsono, ***Advances in Embedded Systems***, Malaysian Book Publishers Association, Skudai 2008, http://www.penerbit.utm.my/bookchapterdoc/FKE/bookchapter_fke15.pdf

2. C. S. Claus, "Zum Einsatz dynamisch rekonfigurierbarer eingebetteter Systeme in der Bildverarbeitung", Technical University Munich, ***Ph.D. Thesis***, 2010, http://deposit.d-nb.de/cgi-bin/dokserv?idn=101123100x&dok_var=d1&dok_ext=pdf&filename=101123100x.pdf

Z. Stamenkovic, K. Tittelbach-Helmrich, M. Krstic, J. Perez, J. Via, and J. Ibanez, "Architecture of an Analog Combining MIMO System Compliant to IEEE802.11a", *Proc. ICT-MobileSummit 2009*, Santander (Spain) 2009, (pp.1-8)

1. M. Yasukawa and T. Saba, "Time-domain ML Channel Estimation Considering Antenna Switching Time for RF-MIMO-OFDM", ***Proc. 7th IEEE GLOBECOM Broadband Wireless Access Workshop,*** Houston (USA) 2011, (pp. 1359-1363), http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6162408

Z. Stamenkovic, E. Miletic, M. Obrknezev, and K. Tittelbach-Helmrich, "MAC Protocol Implementation in RF-MIMO WLAN", *Proc. 16th IEEE International Conference on Electronics, Circuits, and Systems*, Yasmine Hammamet (Tunisia) 2009, (pp.303-306)

1. E. Miletic, K. Tittelbach-Helmrich, and G. Panic, "Performance Investigation on an MIMO-capable 802.11a Compliant MAC Protocol Implementation", ***Proc. 7th International Conference on Mobile Ad-hoc and Sensor Networks***, Beijing (China) 2011, (pp. 190-193), http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=6117412

K. Tittelbach-Helmrich, E. Miletic, P. Wcislek, and Z. Stamenkovic, "MAC Hardware Platform for RF-MIMO WLAN", *Proc. 53rd IEEE International Midwest Symposium on Circuits and Systems*, Seattle (USA) 2010, (pp.339-342)

1. E. Miletic, K. Tittelbach-Helmrich, and G. Panic, "Performance Investigation on an MIMO-capable 802.11a Compliant MAC Protocol Implementation", ***Proc. 7th International Conference on Mobile Ad-hoc and Sensor Networks***, Beijing (China) 2011, (pp. 190-193), http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=6117412

R. Kraemer, Z. Stamenkovic, K. Tittelbach-Helmrich, L. Gonzalez, S. Ruiz, O. Gago, J. Ibanez, V. Elvira, M. Wickert, and R. Eickhoff, "RF-MIMO WLAN Modem Demonstrator", *25th Wireless World Research Forum Meeting*, London (United Kingdom) 2010.

1. V. Elvira, **"**Baseband Processing in Analog Combining MIMO Systems: From Theoretical Design to FPGA Implementation", University of Cantabria, ***Ph.D. Thesis***, 2011, http://www.tesisenred.net/bitstream/handle/10803/32206/TesisVEA.pdf

Z. Stamenkovic, K. Tittelbach-Helmrich, M. Krstic, J. Ibanez, V. Elvira, and I. Santamaria, "MAC and Baseband Hardware Platforms for RF-MIMO WLAN (invited)", *Proc. 5th European Conference on Circuits and Systems for Communications*, Belgrade (Serbia) 2010, (pp.26-33)

1. V. Elvira, **"**Baseband Processing in Analog Combining MIMO Systems: From Theoretical Design to FPGA Implementation", University of Cantabria, ***Ph.D. Thesis***, 2011, http://www.tesisenred.net/bitstream/handle/10803/32206/TesisVEA.pdf

V. Elvira, J. Ibanez, I. Santamaria, M. Krstic, K. Tittelbach-Helmrich, and Z. Stamenkovic, "Baseband Processor for RF-MIMO WLAN", *Proc. 17th IEEE International Conference on Electronics, Circuits, and Systems*, Athens (Greece) 2010, (pp.798-801)

1. V. Elvira, **"**Baseband Processing in Analog Combining MIMO Systems: From Theoretical Design to FPGA Implementation", University of Cantabria, ***Ph.D. Thesis***, 2011, http://www.tesisenred.net/bitstream/handle/10803/32206/TesisVEA.pdf

2. E. Miletic, K. Tittelbach-Helmrich, and G. Panic, "Performance Investigation on an MIMO-capable 802.11a Compliant MAC Protocol Implementation", ***Proc. 7th International Conference on Mobile Ad-hoc and Sensor Networks***, Beijing (China) 2011, (pp. 190-193), http://ieeexplore.ieee.org/search/srchabstract.jsp?tp=&arnumber=6117412

R. Eickhoff, K. Tittelbach-Helmrich, M. Wickert, J. Wagner, U. Mayer, V. Elvira, J. Ibanez, Z. Stamenkovic, and F. Ellinger, "Physical Layer Amendments for MIMO Features in 802.11a", *Proc. Future Network and MobileSummit 2011*, Warsaw (Poland) 2011, (pp.1-8)

1. V. Elvira, **"**Baseband Processing in Analog Combining MIMO Systems: From Theoretical Design to FPGA Implementation", University of Cantabria, ***Ph.D. Thesis***, 2011, http://www.tesisenred.net/bitstream/handle/10803/32206/TesisVEA.pdf

T. Nikolic, M. Stojcev, and Z. Stamenkovic, "Wrapper Design for a CDMA Bus in SOC", *Proc. 13th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems*, Vienna (Austria) 2010, (pp.243-248)

1. B. M. Peiffer, "Design and Verification of Physical Layer Architecture for a 1-Wire Sensor Communication Bus", University of Iowa, ***Master's Thesis***, 2011, http://ir.uiowa.edu/cgi/viewcontent.cgi?article=2438&context=etd

3. MIŠLJENJE O ISPUNJENOSTI USLOVA ZA IZBOR

Uvidom u konkursni materijal, Komisija konstantuje da je kandidat kvalifikovan i da zadovoljava uslove predviđene Pravilnikom o postupku i načinu vrednovanja, i kvantitativnom iskazivanju naučno-istraživačkih rezultata istraživača Republike Srbije za izbor u zvanje naučni savetnik, donetog dana 21.03.2008. god.

U tabeli 1 prikazani su ostvareni rezultati kandidata definisani Minimalnim kvantitativnim zahtevima za sticanje pojedinačnih naučnih zvanja u oblasti tehničko-tehnološke i biotehničke nauke Pravilnika.

Zvanje naučni savetnik	potrebni poeni	ostvareni poeni
kategorije M10+M20+M31+M32+M33+M41+M42+M51+M80+M90≥	54	82
kategorije M21+M22+M23+M24+M31+M32≥	26	29
Ukupno (uključujući kategorije M52 i M34) ≥	70	84

Shodno vrednostima prikazanim u tabeli 1 evidentno je da prijavljeni kandidat svojim rezultatima nadmašuje uslove za izbor u zvanje naučni savetnik.

4. PREDLOG ZA IZBOR KANDIDATA U ODREĐENO ZVANJE

Nakon detaljne i sveobuhvatne analize rezultata svih do sada publikovanih naučnih i stručnih radova sa posebnim osvrtom na kvalitet radova sa SCI liste, aktivnosti na projektima, aktivnosti na uredničkom i recenzentskom radu na većem broju međunarodnih konferencija i u istaknutim međunarodnim časopisima, brojem citiranosti radova, kao i uspešnosti u izvođenju nastave, Komisija predlaže dr Zorana Stamenkovića za izbor u zvanje naučni savetnik za oblast tehničko-tehnološke i biotehničke nauke.

U Nišu, 09.04.2012. god.

Članovi komisije:

Prof. dr Mile Stojčev, s.r.
redovni profesor Elektronskog fakulteta u Nišu

Prof. dr Zoran Prijić, s.r.
redovni profesor Elektronskog fakulteta u Nišu

Prof. dr Milun Jevtić, s.r.
redovni profesor Elektronskog fakulteta u Nišu